1 DESCRIPTION

The MT5721 is an SoC (System on Chip) for magnetic induction based wireless power receiver.

It is fully compliant with the latest WPC Qi specification (Version 1.2.4) of BPP (Baseline Power Profile). It is capable of wireless charging for 5W of delivered power with fully programmable output voltage (maximum 5V) and current limit (maximum 1.2A).

MT5721 has a very high overall AC to DC conversion efficiency (up to 97%), thanks to the optimized and adaptive full synchronous rectifier control, very small Rdson of power MOSFET's, and extremely low bias current.

With the exception of a few external passive components, this SoC integrates everything that is needed for a wireless power receiving function. It is composed of an ARM Cortex M0 processor with 8KB SRAM and 16KB OTP, full synchronous rectifier and special output LDO, robust and reliable over voltage, over current and over temperature protection circuits, bi-directional communication unit and various GPIO's and serial interfaces.

With the flexibility of SoC architecture and the unique implementation, the MT5721 is future proof in supporting WPC Qi specification's further updates and new proprietary protocols.

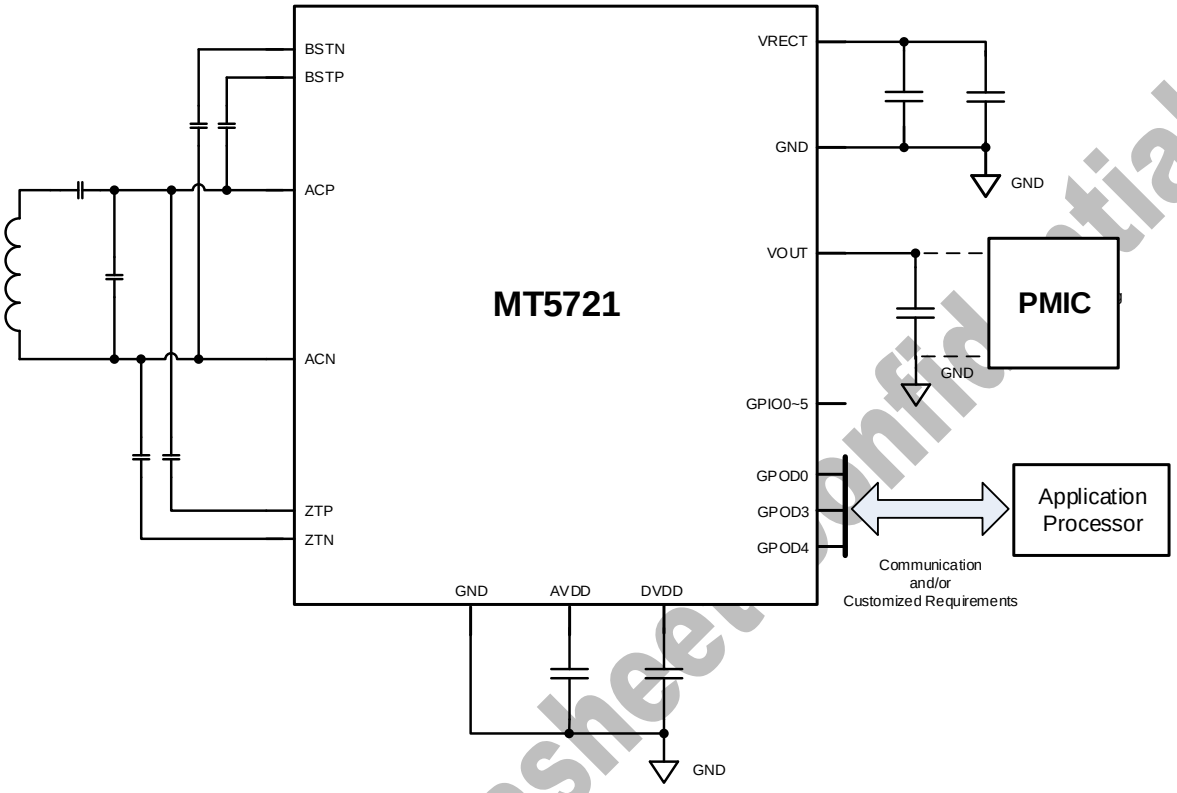
2 FEATURES

- 5W power delivery
- Fully programmable output voltage (up to 5V) and current limit (up to 1.2A)
- Embedded ARM Cortex M0 processor with 8KB SRAM and 16KB OTP
- Up to 97% AC input to DC output efficiency
- Fully integrated bi-directional current sensing
- Reliable and unique over voltage, current, temperature protection
- Specially designed output LDO with output clamping and fast response to line and load transient
- WPC compliant and proprietary communication protocols support with hardware ASK and FSK modulation and demodulation
- Independent I2C slave and I2C master interface with additional GPIO's
- 2.48mm x 3.87mm (6x9 ball array) WLCSP

3 APPLICATIONS

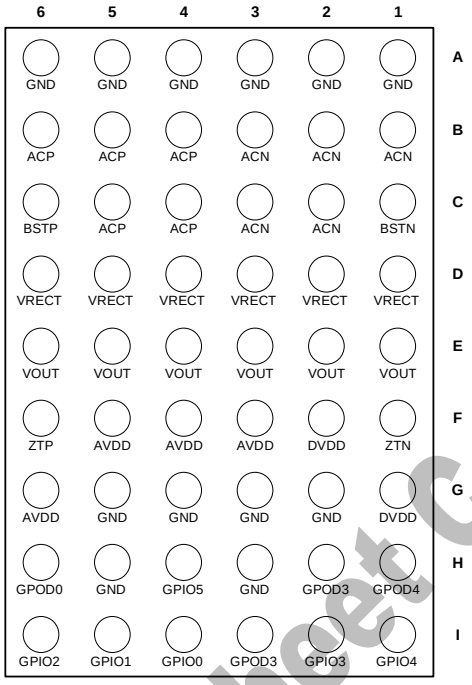
- Standard wireless charging for smart phones with 5W received power
- Wireless charging for wearable devices with high integration and small form factor
- Rx function for phones or power banks where they can be wirelessly charged
- Other wireless power applications

4 TYPICAL APPLICATION CIRCUIT

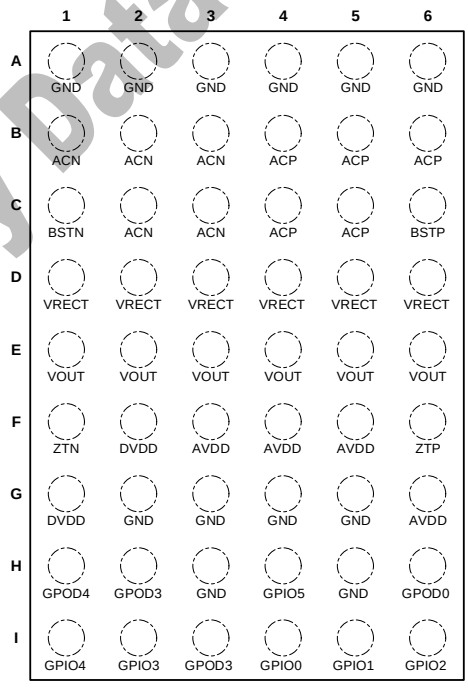


5 PIN CONFIGURATIONS AND FUNCTIONS

5.1 WLCSP Pin Configurations



Bottom View (pin/ball side)



Top View (marking side)

5.2 Pin Functions

Pin Name	Pin No.	Description
ACN	B1, B2, B3, C2, C3	AC input, connect to one end of the coil.
ACP	B4, B5, B6, C4, C5	AC input, connect to the other end of the coil.
GND	A1, A2, A3, A4, A5, A6, G2, G3, G4, G5, H3, H5	Power Ground.
VRECT	D1,D2,D3,D4,D5,D6	Output of Synchronous Rectifier.
VOUT	E1,E2,E3,E4,E5,E6	Output of LDO.
BSTP	C6	Boost Capacitor for internal driver for synchronous bridge rectifier at ACP.
BSTN	C1	Boost Capacitor for internal driver for synchronous bridge rectifier at ACP.
ZTP	F6	ASK Modulation FET at ACP.
ZTN	F1	ASK Modulation FET at ACN.
AVDD	F3, F4, F5, G6	Internal 5V Power Supply.
DVDD	F2, G1	Internal 1.8V Power Supply.
GPOD0	H6	General Purpose I/O. Type: Open Drain. For more details, see Section 5.3.
GPOD3	I3, H2	
GPOD4	H1	
GPIO0~5	I4, I5, I6, I2, I1, H4	General Purpose I/O. Type: Push/Pull. For more details, see Section 5.3.

5.3 I/O Pin Default Configurations

GPOD0, GPOD3, GPOD4	
GPOD0:	Power good. This is to indicate to AP that wireless power is ready.
GPOD3:	I²C slave SCL.
GPOD4:	I²C slave SDA.
Note: GPOD0, GPOD3, GPOD4 can be re-configured upon customer's request.	

GPIO0~5	
GPIO0:	I²C master SCL.
GPIO1:	I²C master SDA.
GPIO2:	General GPIO, ADC.
GPIO3:	General GPIO, ADC.
GPIO4:	General GPIO, ADC.
GPIO5:	General GPIO, ADC.
Note: GPIO0~5 can be re-configured upon customers' request.	

6 SPECIFICATIONS

6.1 Absolute Maximum Ratings

ACN, ACP, ZTP, ZTN	-0.3V to 30V
BSTP, BSTN	-0.3V to ACP+6V, ACN+6V
VRECT	-0.3V to 30V
VOUT	-0.3V to 30V
AVDD	-0.3V to 6V
GPOD0, GPOD3, GPOD4, GPIO0~5	-0.3V to 6V
DVDD	-0.3V to 2V
Storage Temperature	-55°C to 150°C
Maximum Soldering Temperature(Reflow, Pb-Free)	260°C

6.2 ESD Ratings

Test Model	Pins	Ratings
HBM	All pins	(TBD) V
CDM	All pins	(TBD) V

6.3 Recommended Operating Conditions

Operating Temperature(Environment)	-40°C ~85°C
Operating Current (Iout)	0 ~ 1A
Operating Voltage (Vrect)	3.5V ~ 5V

6.4 Thermal Information (Package Thermal Data)

Junction to ambient ($R_{\theta JA}$)	50°C/W

6.5 Electrical Characteristics

(Test conditions: V_{RECT}=12V, T_A=25°C, unless otherwise stated.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up (VDD pin)						
UVLO	Under Voltage Lockout	VRECT rising from 0V		2.95		V
U_{VLO_HYS}	Under Voltage Lockout Hysteresis	VRECT falling		200		mV
Supply Current						
I_q	Quiescent Current			6		mA
Bridge Rectifier						
Rds(on)	Rds(on) of Power MOSFETs			40		mΩ
Over-Voltage Protection						
V_{OVP-DC}	DC Over-Voltage Protection(programmable)	Rising voltage			20	V
LSB_Vovp	Least Significant Bitat OVP			550		mV
LDO						
VOUT	Output Voltage Regulation	Vrect = 8V, Iout = 0A		5		V
LSB_VOUT	Least Significant Bit when programming output voltage			25		mV
Programming _Range				3~5		V
ILimit_max	Output Current Limit				1.2	A
LSB_ILimit	Least Significant Bit when programming output current limit			25		mA
ADC						
N	Resolution			12		Bit
f_{Sample}	Sampling Rate			100		kS/s
Channel	Number of Channels			8		
Miscellaneous						
AVDD	AVDD Output Voltage			5		V
DVDD	DVDD Output Voltage			1.8		V
Digital I/O Pins						
GPOD0, GPOD3, GPOD4	HIGH Level Input Voltage V_{IH}		1.26			V
	LOW Level Input Voltage V_{IL}				0.54	V
	LOW Level Output Voltage V_{OL}			0		V
	LOW Level Output Current I_{OL}	Test at V_{OL}=0.4V	2/8	4.4/17①		mA
	Analog Input Range			0~2.4		V
GPIO0~5	HIGH Level Input Voltage V_{IH}		3.5			V
	LOW Level Input Voltage V_{IL}				1.5	V
	HIGH Level Output Voltage V_{OH}			5		V
	LOW Level Output Voltage V_{OL}			0		V

	HIGH Level Output Current I_{OH}	Test at V_{OH}=4V	2/8	7.8/29①		mA
	LOW Level Output Current I_{OL}	Test at V_{OL}=0.4V	2/8	4.4/17①		mA
	Analog Input Range			0~5		V

Note①: Digital I/O pin output current can be programed.

6.6 Typical Operating Characteristics

The following performance characteristics were taken using MT5815 wireless power transmitter at T_A=25℃, unless otherwise noted.

Figure 1. Efficiency vs. Output Load: Vout=5V

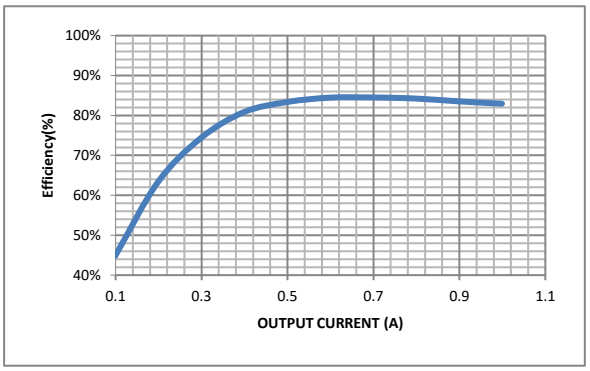


Figure 2. Load Reg. vs. Output Load: Vout=5V

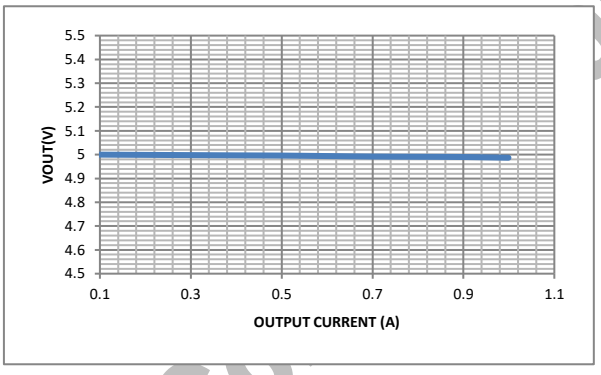
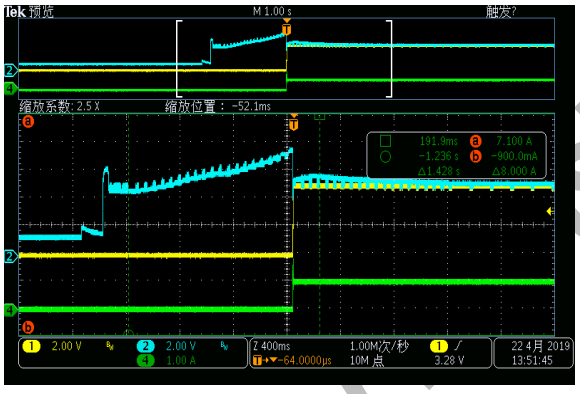


Figure 3. Enable Startup: V_{OUT}=5V; I_{OUT}=1A



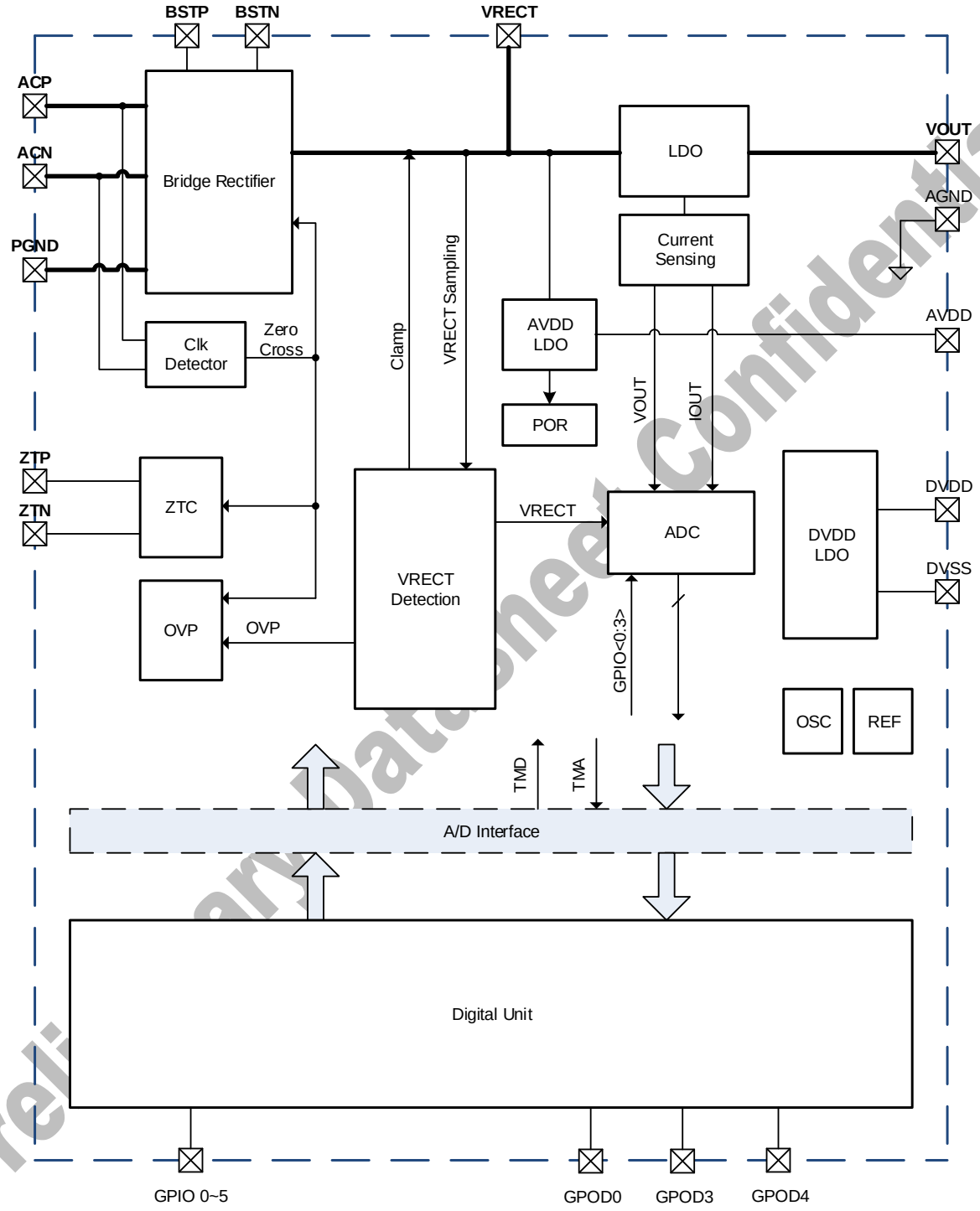
7 DETAILED DESCRIPTIONS

7.1 Overview

MT5721 is an SoC (System on Chip) for wireless power receiver. It only needs several passive components like power receiving coils, resonant tank capacitors, decoupling capacitors and pull up/down resistors to build a complete wireless power receiver system. When coupled with a wireless power transmitter, this system can provide all the functions for wireless power transfer, including power receiving and rectification, output regulation, communication for power control and data exchange, and abnormal condition (over voltage, current, temperature, etc.) protection.

MT5721 is by default programmed to be fully compliant with the latest WPC Qi Specification Version 1.2.4 with support of BPP (Baseline Power Profile).

7.2 Functional Block Diagram



7.3 Theory of Operation

MT5721 is composed of several major functional blocks which together achieve the wireless power receiving function.

Bridge Rectifier, which is also called Full Synchronous Rectifier. This block converts the received AC power from the resonant tank to DC power with the help of the capacitors connected on its output.

LDO, which is also called Main LDO or Output LDO. This block functions as a load switch (connecting and disconnecting the external load), output voltage and current regulation and output clamping when fast load/line transient happens.

AVDD and DVDD LDO and POR. These blocks provide the necessary regulated power supplies from rectifier output for the operation of the chip.

ZTC and CLK Detector. These blocks are for the bi-directional communication for power control and data exchange.

OVP and Vrect Detection. These blocks are for the rectifier output voltage detection and over voltage protection when Vrect is too high.

OSC and REF. These blocks provide the timing reference and voltage reference for the whole chip.

ADC. This block is one of the key blocks that convert various measured analog variables (voltages, currents, temperature, external analog inputs, etc.) to digital domain such that the embedded micro controller can use the information for follow up actions.

Digital Unit. This block contains all the digital circuits, which include embedded micro controller, volatile and nonvolatile memories, I2C interface, peripherals, DMA (Direct Memory Access), internal buses, and other digital functional blocks. This block is the brain of the whole chip which dynamically configures chip for different functions in different state, communicate with the outside world (power transmitter external host), and perform necessary data processing for proper operation (like target Vrect and Vout calculation, etc.)

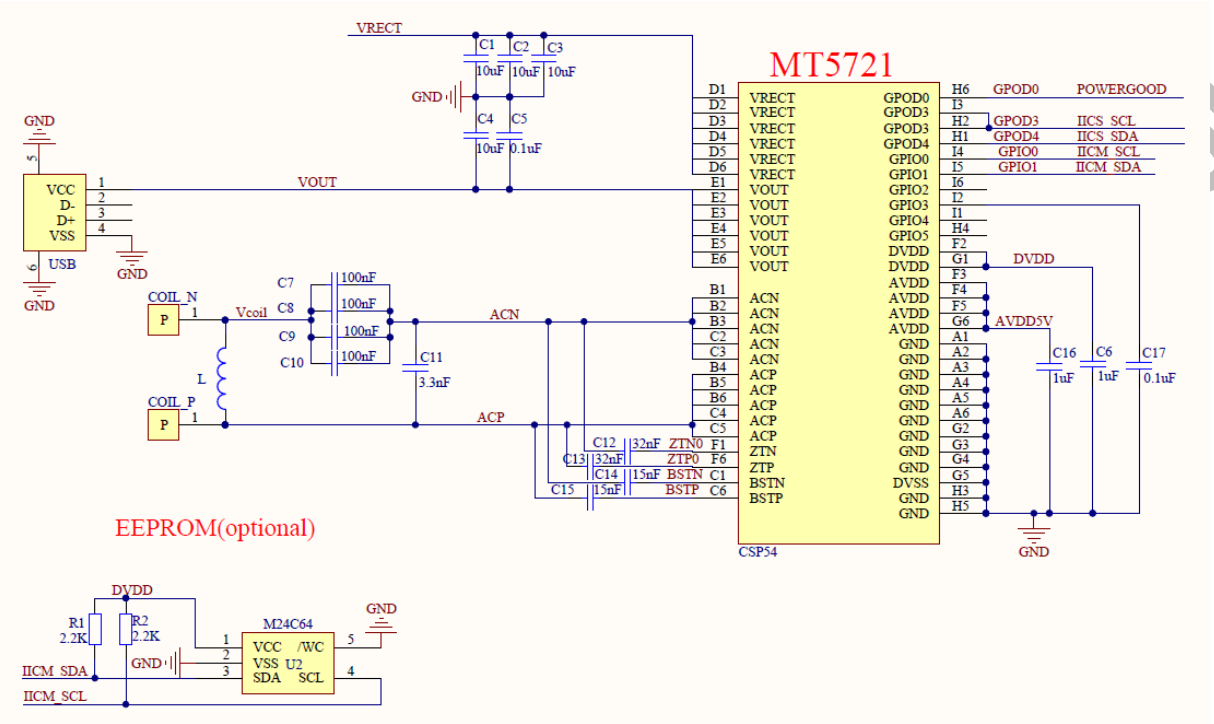
7.4 Device Function Modes

MT5721 can be programmed to operate in different modes. The switching among these modes can be made automatically based on the types of the transmitter or the instruction from the transmitter the receiver is coupled with. The operation modes can also be programmed by an external host (e.g., an Application Processor in a smart phone) via I2C interface. Here are some of these modes:

- WPC BPP only receiver mode
- WPC BPP and proprietary receiver mode
- WPC proprietary only receiver mode

8 APPLICATIONS AND IMPLEMENTIONS

8.1 Reference Schematic



8.2 BOM

#	Reference	Value	Description	Footprint	Quanti
1	R1, R2	2.2K	RES SMD 2.2K 5% 1/20W	0201	2
2	C1, C2, C3, C4	10uF	CAP CER 10UF 16V X7R 0603	0603	4
3	C5	0.1uF	CAP CER 0.1UF 16V X7R 0603	0603	1
4	C6, C16	1uF	CAP CER 1UF 6.3V X7R 0201	0201	2
5	C7, C8, C9, C10	100nF	CAP CER 0.1UF 25V X7R 0603	0603	4
6	C11	3.3nF	CAP CER 0.0033UF 25V X7R	0402	1
7	C12, C13	32nF	CAP CER 0.032UF 25V X7R 0402	0402	2
8	C14, C15	15nF	CAP CER 0.015UF 25V X7R 0402	0402	2
9	C17	0.1uF	CAP CER 0.1UF 6.3V X7R 0201	0201	1
10	U1	MT5721	Wireless power receiver	CSP54	1
11	U2	M24C64	EEPROM	UFDFP	1
				Notes	21

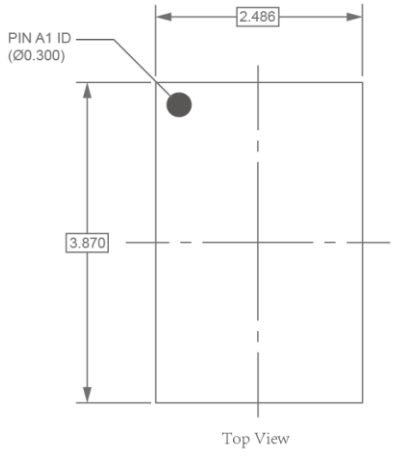
9 DETAILED PACKAGING INFORMATIONS

WLCSP Package Outline and Dimensions

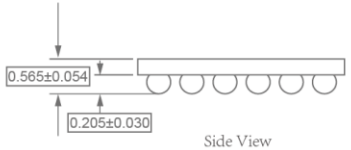
REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	2018/12/04	

NOTES:

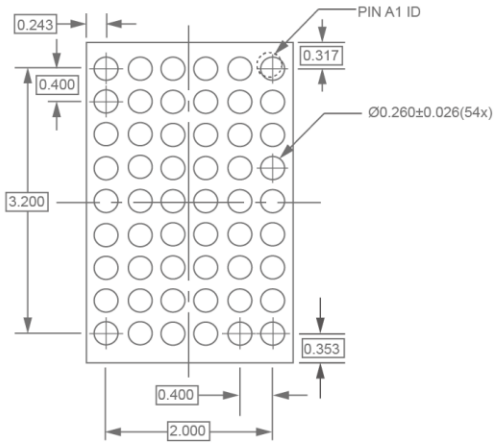
1. ALL DIMENSIONS AND TOLERANCES ARE PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.



Top View



Side View



Bottom View

		www.maxictech.com TEL:010-62662828
APPROVALS	DATE 2018/12/04	TITLE WLCSP54 PACKAGE OUTLINE 2.486 x 3.870 BODY 0.4mm PITCH DSBGA
REVISION 00	DO NOT SCALE DRAWING	SHEET 1 OF 1

10 ORDERING INFORMATION

Part No.	Package Type	Package Information	Package Quantity	Ambient Temperature	Chip Mark
MT5721	WLCSP	2.48 x 3.87mm 54-WLCSP	3000	-40°C~+85°C	MT5721 YYWWXX XXXX

11 REVISION HISTORY

Revision	Date	Description
1.0	2019-04-19	Preliminary version.

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